EFFECT OF INTEGRATED CIRCUITS ON SYSTEMS - COMPARATIVE CASE

by Robert Ricks

INTRODUCTION

When integrated circuits (IC's) were first introduced, one of the startling effects was the reduction in system size made possible by the changeover from discrete devices to microcircuits. Today, the comparison is even more radical, not only from the point of system size, but from the degree of increased circuit complexity, reduction in can count, and demonstrated compatibility of Fairchild IC families.

For further comparison of these relative merits, an example case of one of the first digital frequency meters (DFM)* is discussed in relation to equivalent metering systems where second generation IC's are substituted for the introductory, or first generation IC's.

OPERATIONAL PRINCIPLE OF DIGITAL FREQUENCY METER

Frequency and time can be measured with the greatest accuracy by digital techinques. The digital frequency meter considered here operates on this basic principle. The DFM accepts signal inputs over an unusually wide frequency range and wide impedances, then measures and numerically displays these events per unit time.

MEASURING TECHNIQUES

Several types of measurements can be made by selecting appropriate values for the two variables, frequency and time; the most important being the measurement of frequency, period, and time interval between two signals. The relevant configurations are called the frequency meter, period meter, and chronometer, respectively.

* Developed by Fairchild's SGS using RTμL integrated circuits (Resistor-Transistor Logic).

Fundamentally, all configurations are obtained by means of a control gate, whose output is connected to a counting circuit, which in turn is linked with a numeric display system. The unit has auxiliary equipment such as input circuits and control circuits.

Each measurement is in practice a ratio between the two main variables, one of which is the function to be measured; the other, the time base, must be very precise and within a selected convenient range. This T. B. is achieved by means of a crystal-controlled oscillator, followed by decimal division decades. Furthermore, the operational sequence is appropriately programmed by means of the control circuits, since most of the measurements are periodic. Finally, the connections are modified through manually operated selector and rotary switches, since all configurations use the same basic circuits.

Frequency Measurement (Frequency Meter)

An unknown frequency is measured by counting the number of cycles over an interval of time which will be referred to as T. B. (time-base). The number of cycles counted after they have passed through the control gate depends on the T. B. value and is, by definition, the frequency measured (cycles, kilocycles, or megacycles) when the T. B. is equal to 1 second, millisecond, or microsecond, respectively.

Period Measurement (Meter-Multiperiod Meter)

The period of a function is measured by counting the pulses coming directly from the crystal oscillator or from frequencies which are submultiples of the oscillator in powers of ten, while the conditioning signal is the period of the fre-

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quency to be measured, or a decimal submultiple of that frequency.

Thus, two types of measurement are possible, depending upon which signal engages the divider. Then the oscillator pulses engage the divider, the configuration is a period meter, and the result of the count gives the period directly in microseconds, milliseconds, or seconds when the frequency of the pulses counted is 1 megacycle, 1 kilocycle, or 1 cycle per second, respectively. When the function to be measured is routed to the divider, the multiperiod meter multiplies the period in powers of 10 and then counts with pulses direct from the oscillator.

Chronometer

An interval of time between "start" and "stop" pulses is measured either by counting the pulses direct from the oscillator or through decimal divisions. Thus, two inputs must be provided: the control gate must be opened by the signal from the first input and closed by the signal from the second; and the number of pulses counted should give the time-interval directly. These two signals can be generated internally or externally by corresponding "manual" or "automatic" settings.

TEST POSITION

The DFM can also control the exact operation of all circuits directly without resorting to external frequencies by a special connection-enabling pulse from the oscillator to be counted during the time-interval generated by the oscillator. In the event of a positive test, the number 10^5 will be displayed on the numeric indicators.

The selector switch can be set to substitute external standard frequency for the internal frequency by a special input designated F_C. The degree of accuracy and the extent of the measurement are dependent on the precision of the external frequency.

COMPARISONS OF FIRST AND SECOND GENERATION SYSTEMS

INPUT CIRCUITS

First Generation

As shown in Figure 1, each input circuit in the first generation input circuit is made up of an amplifier, a trigger, and an inverter. The working frequency can vary from zero to 10 megacycles per second; the minimum input signal is about 100 millivolts up to 1 cycle per second and two to three times higher over the remaining frequency range; the maximum input signal can change between +4 volts and -4 volts.

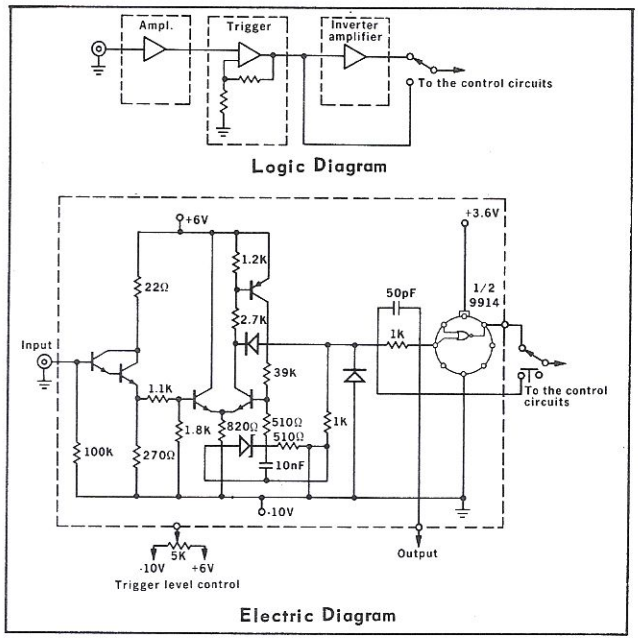

Fig. 1. Logic and electric diagrams.

The amplifier, formed by two NPN transistors, has unity gain and input impedance equal to 100 kilohms with approximately 10 picofarads in parallel. The trigger, consisting of two NPN transistors and one PNP transistor, has provisions for manual threshold selection.

The inverter is half a medium-power RTμL element, the 9914, and its output is one of the two inputs to a selector switch, the other input being that of the trigger. Thus, in the chronometer configuration, the DFM is able to synchronize itself both on positive and negative transitions of the input signals. This characteristic enables the duration of a signal to be measured (e.g., the output of a monostable circuit) by sending it to both F_A (start) and F_B (stop) channels and making channel F_A sensitive to the first transition of the signal, and channel F_B sensitive to the second transition.

Second Generation

As seen in Fig. 2, each DFM input circuit using second generation IC's consists of a Fairchild 2N4360 low drain-to-

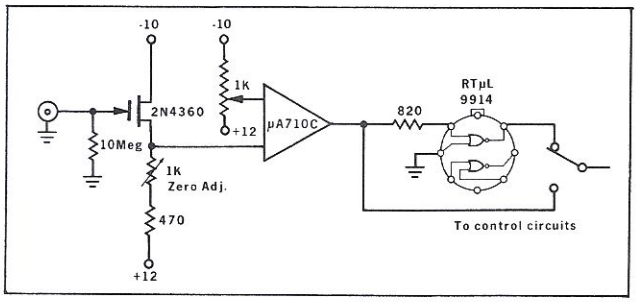

Fig. 2. Second generation digital frequency meter input circuitry.

source resistance field-effect transistor (FET) driving a Fairchild μA710C differential comparator.

The balance potentiometer in the FET input circuit is accessible from the front panel to provide external dc offset adjustment.

TABLE I.

INPUT CIRCUITRY COMPARISON.

1st Gen. (Figure 1)	2nd Gen. (Figure 2)
5 transistors 13 resistors 2 capacitors 2 diodes 1 potentiometer 1/2 9914 gate	1 2N4360 3 resistors 1 μA710C 2 potentiometer 1/2 9914 gate
Total 23 components plus gate	7 components plus gate

Table I is a comparison of the physical configurations and Table II shows the DFM system performance incorporating the undated IC technology compared with that using first generation IC's.

TABLE II.

SYSTEM PERFORMANCE COMPARISON.

Parameters	1st Gen.	2nd Gen.
Frequency	dc to 10 MHz	dc to >10 MHz
Threshold	100 mV to 300 mV (at 1 MHz)	5 mV
Common Mode Range	-4V to 4V	-5V to 5V
Input Impedance	100k in parallel with 10 pF	>5 M in parallel with 5 pF

DIVIDER CIRCUITS

First Generation

The first generation divider circuit (Fig. 3) consists of six cascaded decimal counters. Each counter is made up of four 9926 elements and the decimal count is obtained using the JK logic properties without having to resort to external gating.

The first input signal to the divider causes a change in all the decades and generates the T. B. signal in the configuration in which the T. B. generator is controlled by the divider. The need for this feature is to synchronize the T. B. with pulses starting the measurement.

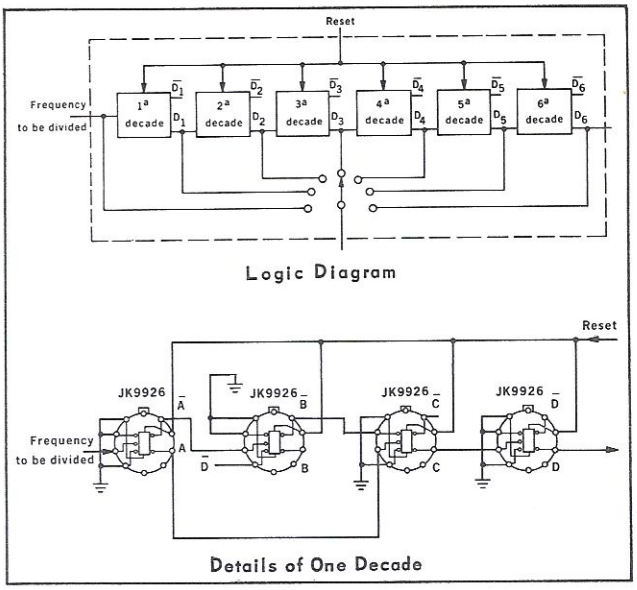

Fig. 3. Logic diagram of divider with details of one decade.

Second Generation

The newest divider circuit (Fig. 4) consists of six cascaded decimal counters in the same logic configuration as the one shown in Fig. 3. The first decade uses four interconnected 9926 JK flip-flops to reduce the frequency of operation to a maximum of 1 megahertz for the five CμL 9958 integrated decade counters which comprise the next five stages of the decade string.

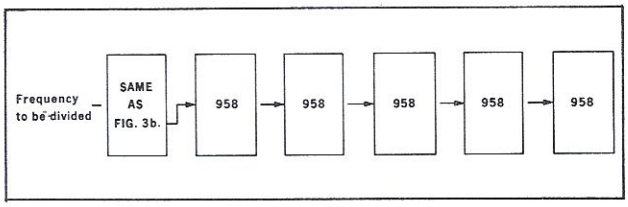

Fig. 4. Logic diagram of second generation divider circuit.

Comparison of Divider Circuits

Table III below is a comparison of the number of elements in the old and new divider circuits.

TABLE III.

DIVIDER CIRCUITRY COMPARISON.

1st Generation	2nd Generation
24 JK flip-flops	5 CμL 9958's 4 JK flip-flops

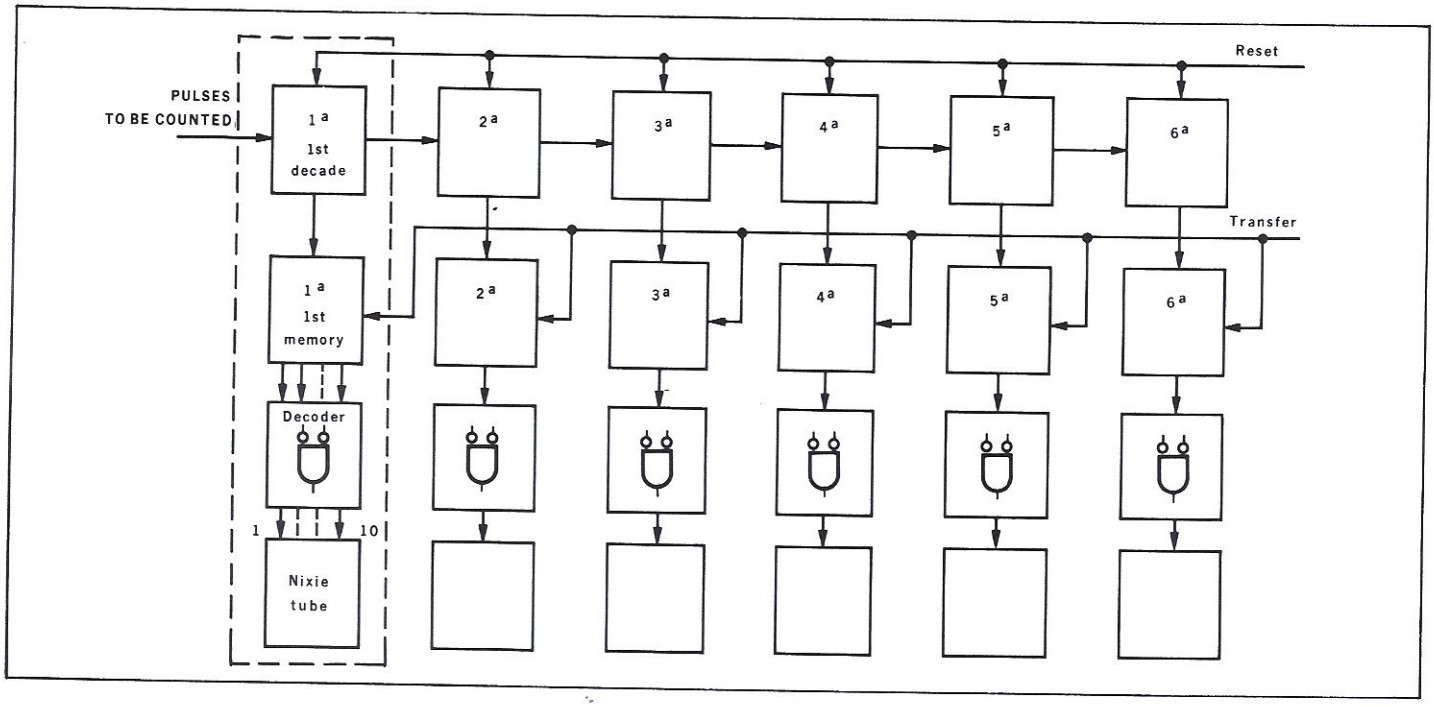

Fig. 5. Logic diagram of counter.

COUNTER CIRCUITS

First Generation

The first generation counter depicted in Figs. 5, 6, and 7 consists of six Johnson-type cascade-connected, decimal counters, each one made up of five 9926 JK flip-flops. Five 9905 elements per stage are used as gated temporary memories for the contents of the decade counters. The typical counting speed is approximately 10 megacycles per second.

The binary information is converted to decimal by a matrix, formed by five RTμL 9914 devices, whose output signals control the gas-filled numeric indicators through high-voltage transistors.

Second Generation

The second generation counter (Fig. 8) consists of the same layout as the updated divide circuit with the input stage using the RTμL9926's and the remaining lower frequency stages using the CμL9958 integrated decade counters. The stored count is then transferred by the application of the transfer signal into the CμL9959 buffer-storage elements. Both the binary-to-decimal decoding and the direct gas-filled numeric indicators driving functions are performed by the CμL9960 decoder-driver to complete the counter operation.

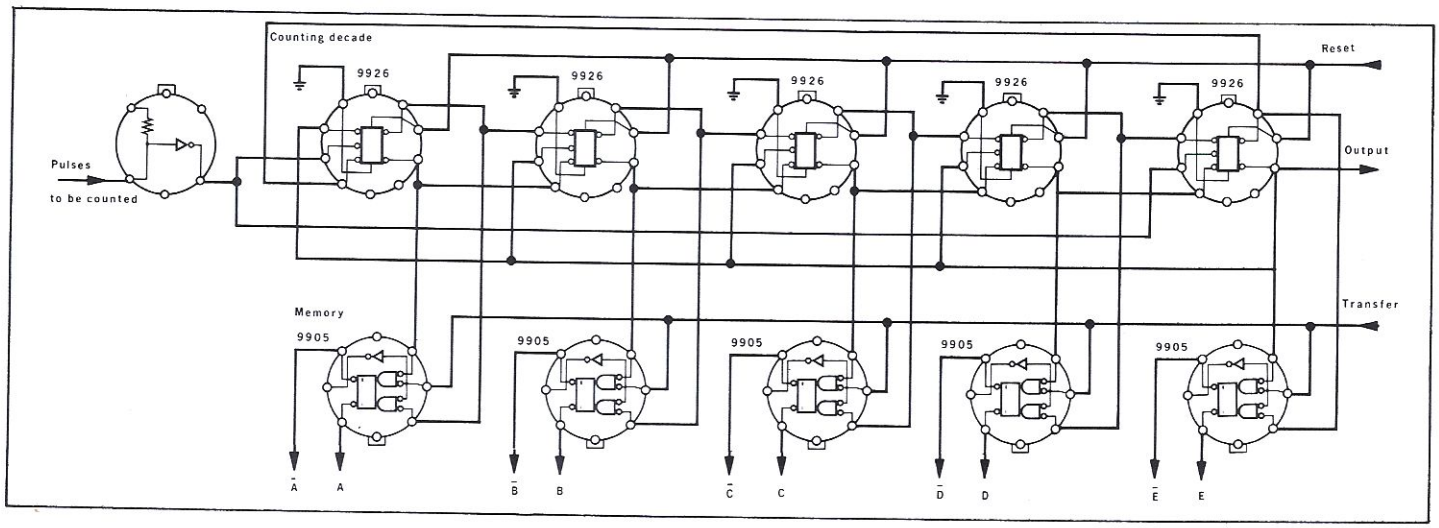

Fig. 6. Counting decade with memory.

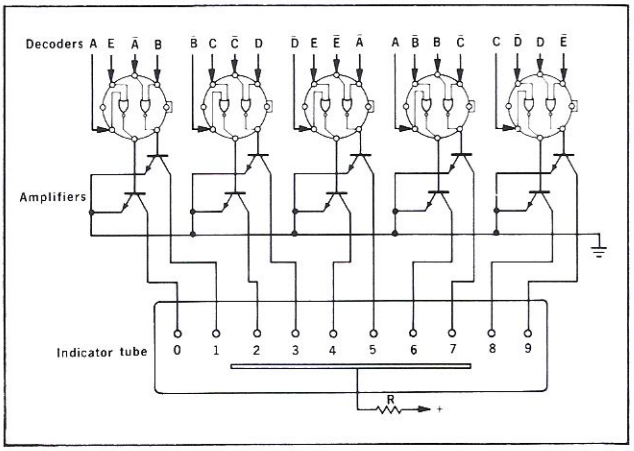

Fig. 7. Decoding matrix with voltage amplifiers and gas filled indicators.

Comparison of Counter Circuits

A comparison is made in Table IV below of the two counter circuits just described.

TABLE IV.

COUNTER STORAGE AND DISPLAY COMPARISON.

Function	1st Generation	2nd Generation
Counter	30 JK flip-flop	5 CμL 9958's 4 JK flip-flops
Storage	30 RTμL9905's used as memory elements	6 CμL 9959's
Decoding and Driving	30 RTμL 9914's 60 high-voltage transistors	6 CμL 9960's
Total	21 cans	150 cans

CONTROL CIRCUITS

The main operations involved in repetitive measurements are:

(a) generation of the T. B. signal to initiate counting pulses through the decade counters;

(b) transfer of results to the memory when the count is completed and production of visual display of results;

(c) setting the computation counters at zero with the memory cut out;

(d) starting a new sequence after any chosen time-interval, if the previous cycle has had time to complete itself; or automatically starting at the end of the precious sequence, if the T. B. is longer than the selected recurring cycle.

The control circuits are made up of four main components as outlined below and described in more detail in the following sections.

(a) A T. B. generator capable of blocking itself and its control signals, after having generated a signal;

(b) A timer, which initiates the various transfer and zero-setting signals, starting at the end of the T. B. and automatically blocking itself;

(c) A pulse generator with a cycle time varying between 0.4 and 5 seconds, approximately, which controls the "sample rate"; i. e., the recurring measurement cycle;

(d) A synchronizer which allows the control pulses to the T. B. generator and can initiate the previously described dual operation.

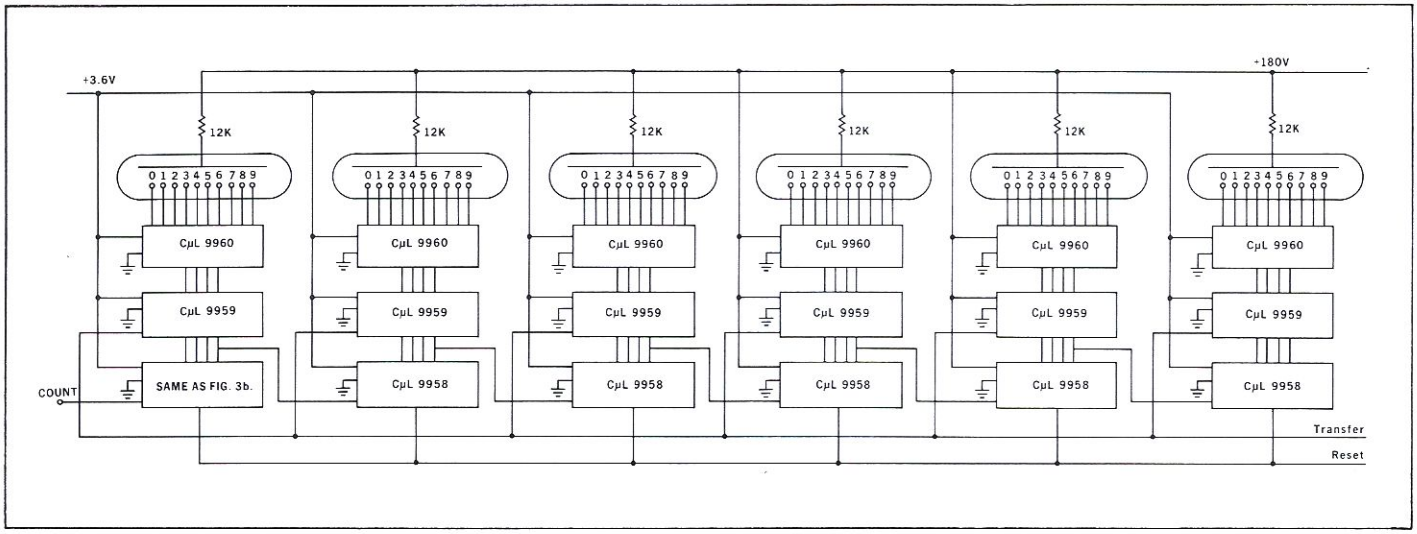

Fig. 8. Second generation counter.

DESCRIPTION OF CONTROL CIRCUITS

"Time-Base" (T.B.) Generator

This consists of two RTμL9926 elements; the first controlled by the signal whose period constitutes the "Time-Base" and the second controlled by the first, so that when the T. B. signal is over, it changes state and blocks both the elements and the input pulses at the control gate; otherwise transient disturbance would be caused on the first of the two elements.

Timer

This consists of a divide-by-four preceded by a gate that governs the passage of control pulses and is followed by a decoding system which generates the various control signals in sequence.

The counter is made up of two 9926 elements and is so designed that, at the end of each sequence, it locks itself in a state which is not decoded, so that the decoding signals are only present when the timer is operating.

The T. B. generator blocking signal opens the gate which controls the timer control signals coming direct from the crystal oscillator or from F_C.

The generated signals, obtained through NOR gates with two or three inputs, have the following sequence:

(1) time 1	transfer to the memory
(2) time 2	zero-setting of the division and counting decades
(3) time 2 - 1st part	interrogation pulse sent to the synchronizer
(4) time 2 - 2nd part	zero setting of the synchronizer memory
(5) time 2 - 3rd part	zero setting of the timer

The control circuit is completed by 9900 elements which are used for signal amplification. Furthermore, in the "manual chronometer" position the timer and the synchronizer are blocked, and the transfer signal is continuously generated so as to obtain a continuous connection between counting decades and decoding matrix.

Finally, the zero-setting signal can be manually achieved by means of the "zero" push button.

Pulse Generator

The pulse generator, for which period T can be continuously varied between about 0.4 and 5 seconds by means of a control outside the instrument, is made up of a multi-

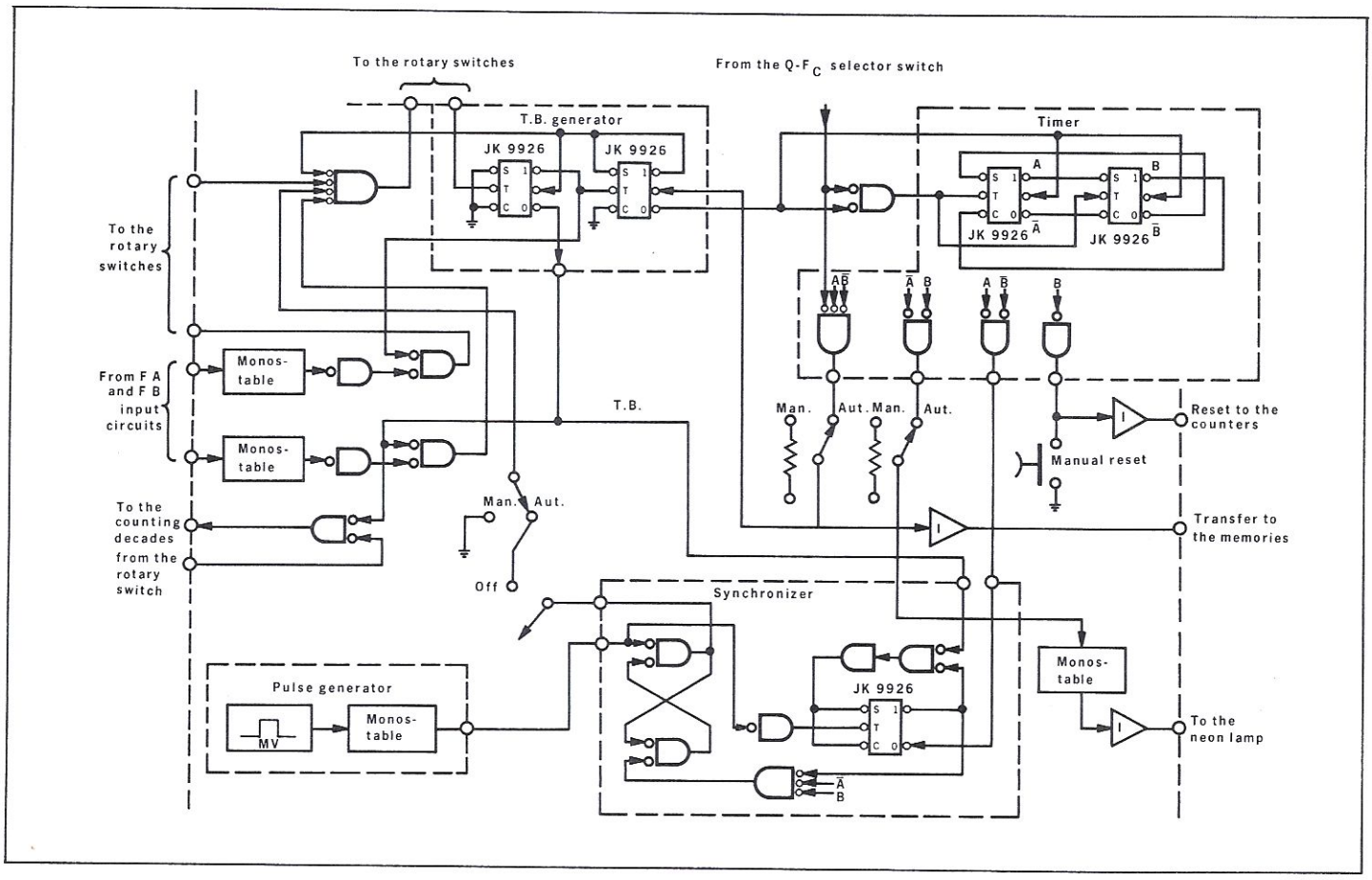

Fig. 9. Logic diagram for control circuits.

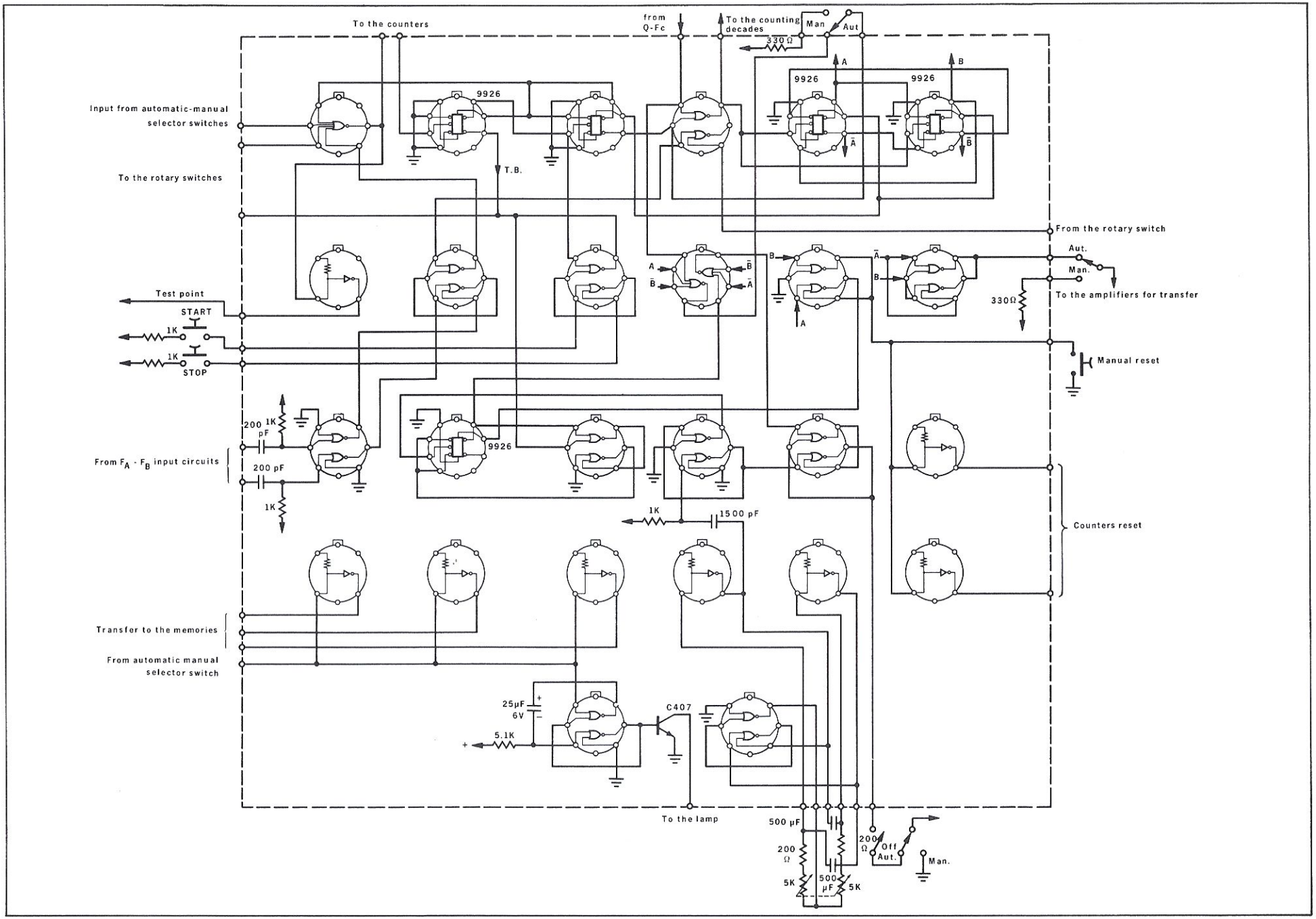

Fig. 10. Circuit diagram of the control circuits.

vibrator and a differentiator with the use of three 9900 elements plus one 9914 element.

Its purpose is to allow the choice of the "sample rate"; otherwise the result of measurement made at short intervals would be difficult to read because of the flickering of the display.

Synchronizer

A chosen repetition period may be right or wrong according to the T. B. value used for the measurement. If this value is greater than the chosen period, a second measurement cannot be started before the previous one has ended. The new measurement then commences at the end of the previous one whose total length is the T. B. plus four service signals which, in the case of the internal crystal frequency (1 Mc/s), takes 4 microseconds. Conversely, when the T. B. is shorter than the chosen period, the instrument is blocked at the end of each sequence, and is unblocked by the synchronizer pulses.

The synchronizer is formed by a two-input bistable circuit, which supplies the conditioning signal to the control gate of the T. B. pulse generator, and by a bistable circuit with conditioned inputs.

The latter consists of one 9926 element, and can only change state when pulses arrive while the T. B. signal is present. The interrogation pulse, generated in the first part of time 2 of the timer, checks whether or not the element has changed state.

In the first case (T < T. B.), no zero-setting pulse is generated for the bistable circuit. Thus, at the end of the sequence, the control gate does not prevent the passage of control pulses to the T. B. generator and enables a new computation operation to be started.

In the second case (T > T. B.), the bistable circuit is reset and the pulses are blocked until a new synchronism pulse arrives.

A manual control can, however, be used to prevent synchronism pulses from operating, with the result that the repetition period is then determined by the T. B. independent of its value.

The visual display of the repetition period is obtained by a neon lamp controlled through a monostable circuit, by the transfer pulses to the memory.

Figures 9 and 10 show the logic and control circuit diagrams.

CONCLUSION

In the rapid technological advance of the semiconductor industry, step-by-step improvements (which separately seem relatively insignificant) will represent a significant total improvement in system configuration and performance after a period of months or a few years. (Refer to Table V below).

TABLE V.

SUMMARY: COMPARISON OF DEVICES IN SYSTEMS.

Circuit	1st Generation	2nd Generation
Input Circuitry	23 components plus gate	7 components plus gate
Divider	24 JK flip-flops	5 CμL 9958's 4 JK flip-flops
Counter	30 JK flip-flops	5 CμL 9958's 4 JK flip-flops
Storage Decoder and Driver	30 RTμL 9905's 90 cans	6 CμL 9959's 6 CμL 9960's
Total cans	197	37
Total Timing and Control Cans	44	44
Total System Cans	241	81

The updated circuitry of the second-generation devices also require less total power as shown in the tabulation below.

TABLE VI.

COMPARISON OF DFM POWER REQUIREMENTS.

DFM	1st Generation	2nd Generation
Total Power Required	7.47 watts	2.48 watts

In the case of the digital frequency meter discussed in this paper, the results after approximately 18 months progress and the increased use of integrated circuits show a marked change in system size and electrical characteristics. (Tables V and VI.) The total number of cans in the counter, storage, decoding and driving circuits have been reduced 140 percent. The overall reliability of system performance is assured by the built-in compatibility of the several microcircuit families.